DESIGN OF LOW POWER 10T SRAM CELL USING ADIABATIC LOGIC

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Abstract

In this research, we analyze and construct Static Random Access Memories (SRAMs) with latency and power efficiency as primary goals. A single CMOS SRAM cell has low power requirements and fast read/write speeds. A more stable and faster read/write process is possible with higher cell ratios. A narrower PMOS transistor consumes less power. In this work, a 6T SRAM cell is built that significantly cuts down on power consumption, latency, and read/write times. When adding more memory, the bit-line parasitic capacitance rises, which causes voltage sensing to take longer. To prevent this issue and boost design speed, apply efficient scaling strategies..

Keywords: Six transistor SRAM, Delay, Power, Aspect ratio.

Introduction

These days, low power SRAMs are an integral part of many VLSI circuits. The on-chip cache sizes of microprocessors are improving with each generation to compensate for the widening gap between processor and main memory speeds [P. Barnes2010, S. Hesley, et al., 2009]. The increasing rise of battery-operated gadgets, together with the greater integration and running speeds, have made power dissipation a crucial factor.

A static random access memory (SRAM) layout serves two functions: Two of its primary uses are to replace DRAMs in systems with stringent power constraints and to offer a direct interface with the CPU at rates that DRAMs cannot match. The primary function of the SRAM is to act as cache memory, communicating with the CPU and DRAMs. The second factor propelling SRAM development is the need from low-power uses. InBecause DRAM refresh current is several orders of magnitude more than low-power SRAM standby current, SRAM are often employed in portable devices.

When we originally began working on the design of SRAM, one of our primary goals was to reduce the required operating voltage from 3V to 1.8V. The second is to lessen the load on the battery by cutting down on static and active power use. However, it has been shown that a drop in supply voltage (Vdd) has a significant impact on memory stability [Evelyn Grossar, 2006]. These objectives may be met by enhancing the pre-charge circuitry and optimizing the memory's aspect ratio. Cell ratios of 1.5–2 and pull-up ratios of less than 1.8 are required for reliable SRAM functioning. According to [Jan M. Rabaey 2003], these proportions are typical for 0.25u equipment. To get the necessary performance, 0.18u technology adjusts this ratio. One novel approach is employed to lessen the load on the memory cell. Some additional work has been published in the literature [Kenneth W.Mai, 1998, K.Takeda et al., 2006] for low power and High Speed SRAM, but [Stefan Cosemans 2007] discusses the approach in detail. However, most efforts are put towards improving the speed and minimizing the power consumption of the peripheral

circuits. First, it presents the design of a 6T SRAM cell using traditional bit-lines; next, to cut down on power consumption and delay, it illustrates a 6T design using a short buffered bit-line. Finally, the work properly measures cell stability.

Methdology

When compared to a 4T resistive load cell, the six MOSFETS that make up a CMOS SRAM cell have a lower power consumption in standby mode and a higher resilience to transient noise and voltage fluctuation. Both 0 and 1 are stable states for the storage cell. During read and write operations, a storage cell's access is managed by four transistors, two inverters, and two access transistors. The cell's connection to the bit lines (BL and BLB) is activated by the word line (WL), which in turn controls the two access transistors (M5 and M6). While having two bit-lines is not technically required, a global bit-line design may assist keep the cell stable and lower the voltage swing, both of which have an initial effect on the cell's power consumption. One other benefit is that it simplifies the SRAM cell.
The inverters in an SRAM cell actively drive a differential sensing amplifier at the end of the bit-line high and low during read access, hence this circuitry is necessary. As a result, SRAM bandwidth is enhanced in comparison to DRAMs. Small voltage fluctuations are more readily detected because to the differential signalling made possible by SRAM's symmetrical structure.
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There are three distinct cellular states:

Waiting: a dormant circuit

Word line inactivity causes M5 and M6 to cut off the cell's connection to the bit lines, but as long as both inverters are powered, they will reinforce each other.

Notice: Information is needed

Both the bit lines and the word lines are active high, therefore the notion of pre-charging is crucial. The addition of a sensing amplifier at the cell's output will eliminate the occasional minor delta delay across the bit lines. When the sense amplifier's sensitivity is increased, data may be read more quickly.

Writing: Updating the contents

The bit-lines are set to the same value regardless of what we're trying to write. Cross-coupled inverters' prior state may be readily overridden by designing bit-line input drivers to be far more powerful than the comparatively weak transistors in the cell itself. To achieve appropriate functioning, an SRAM's transistors must be meticulously sized

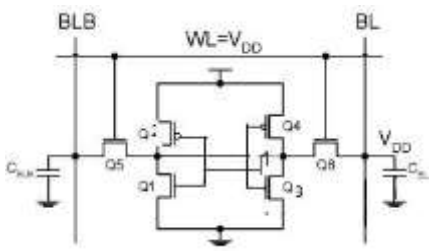

Fig. 1: 6T SRAM cell.

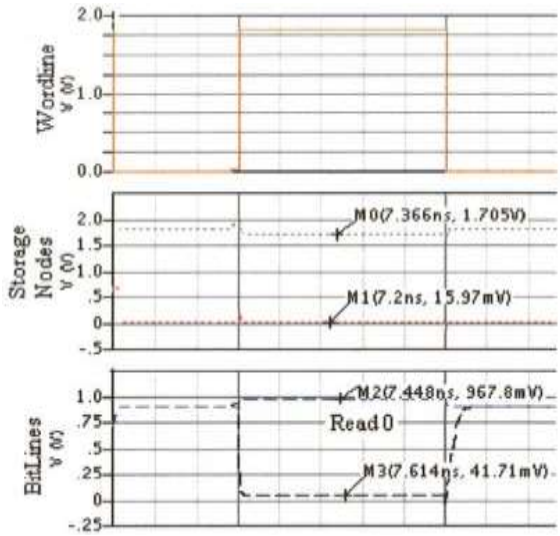

Fig 2: Read Operation

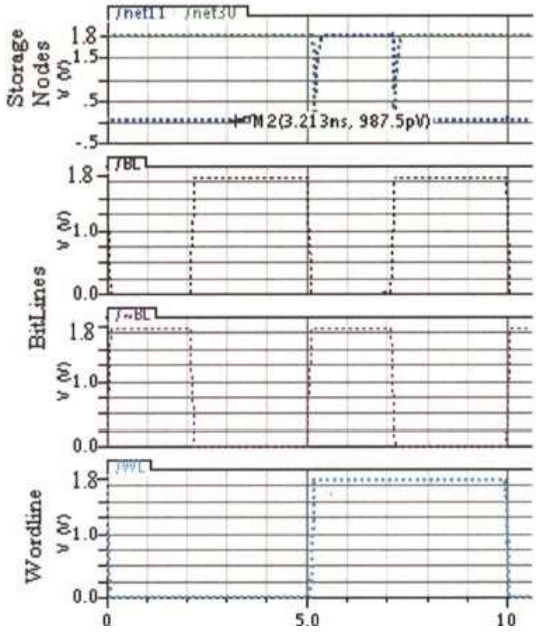

Fig. 3: Write Operation.

Minimal latency, power consumption, and a shiftable aspect ratio (W/L) all need optimal size [K. Itoh 2006, A.P. Chandrakasan et al. 2009]. Capacitance variations have also been used for delay analysis..

Results

Stable The primary goal of cell design is still the preservation of information, and this is achieved by adjusting the aspect ratio of each transistor's gain factor. Lowest delay and lowest power consumption are achieved by adjusting capacitance values and aspect ratio..

Table 1: Simulation results after varying aspect ratio keeping capacitance constant

Aspect ratio of MOSFET		Effect on parameters	
NMOS (W/L)	PMOS (W/L)	C_{cap} Value	Delay Factor(t_d)
1 µ	2 µ	1pf	0.025ns
2 µ	4µ	1pf	0.021ns
4 µ	8 µ	1pf	0.016ns

Table 2: Effect of capacitance variation on Delay factor.

NMOS (W/L)	PMOS (W/L)	C_{cap} Value	Delay Factor
1 µ	2 µ	5pf	0.011ns
4 µ	8 µ	10pf	0.009ns

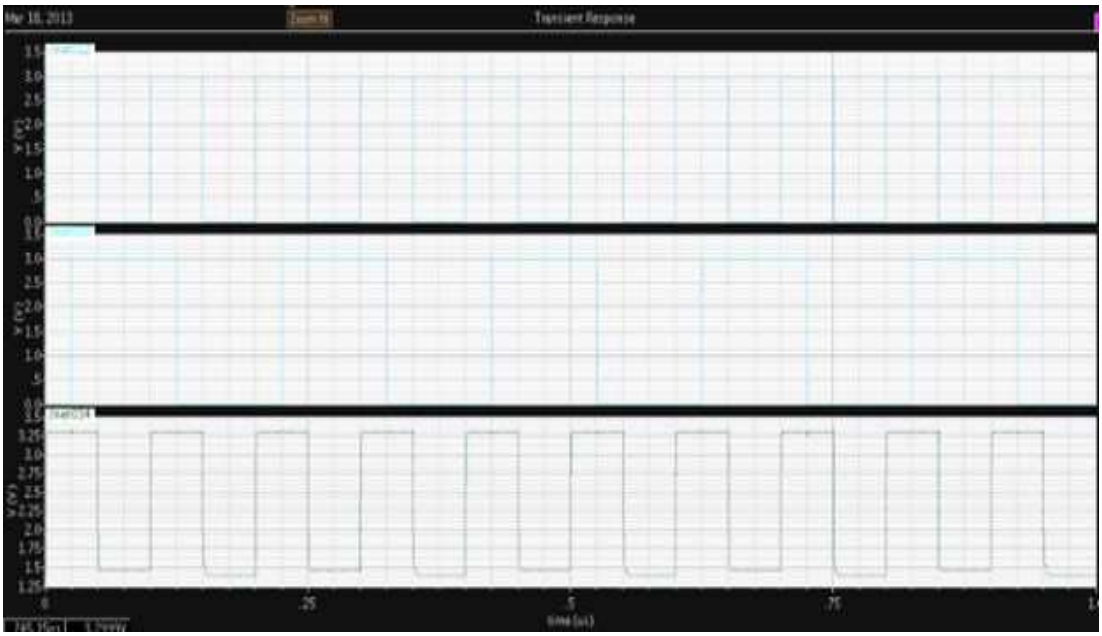

Fig. 4: Waveform of the cell.

Conclusion and Future Scope

Small voltage fluctuations on the bit-lines during the write operation are one of the ways the SRAM achieves its high speed functioning while using little power. Changing the cell such that it functions as a latch type sensing amplifier helps to minimize power consumption and delay by amplifying and storing the little swing write data displayed on the bit-lines.

Parameters	Result from Literature survey[x]	Result obtained from Proposed design
Process Technology	0.25um	180nm
Power supply voltage	2.5v	1.8v
Pre-charge voltage	0.9v	1v
Power consumption	3.4mW	3.146mW
Delay	3.4ns	2.ns

[x]Results are taken from the design described in[Bharadwaj S. Amrutur 1999].

Delay and power consumption in SRAMs will scale with their size and technology. Various design options are investigated using simple analytical models for delay.
Future energy efficiency will be greatly aided by lekage current. The size of the cell may be decreased by using the cadence tool's standard library to design a layout for one's own transistors.

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